

TEST RELIABILITY AND SECURITY CHALLENGES IN VLSI SYSTEMS

CALL FOR PAPERS

The IEEE VLSI Test Symposium (VTS) explores emerging trends and novel concepts in test, reliability, calibration, validation, yield, and security of microelectronic circuits and systems. The VTS Program Committee invites original - unpublished paper submissions for VTS 2026 Proposals for the innovative practices and special session tracks are also invited.

Major topics include but are not limited to:

- Generative AI Applications in Test & Security
- Silicon Lifecycle Management
- Silent Data Corruption
- Test-Enabled Digital Twin
- Analog - Mixed-Signal - RF Test
- ATPG & Compression
- Automotive Test & Safety
- Built-In Self-Test (BIST)
- Functional safety
- Digital Twin Enabled Test & Security
- High BW Test through High-Speed Interfaces
- Testing for Extreme Environments
- Test for Non-Si & Compound Circuits
- On-Line Test & Error Correction
- Power & Thermal Issues in Test
- System-on-Chip (SOC) Test
- Test & Reliability of Biomedical Devices
- Test & Reliability of High-Speed I/O
- Test Standards
- FPGA Test
- Defect-Based Test
- Defect & Fault Tolerance
- Delay & Performance Test
- Design for Testability
- Post-silicon Validation & Debug
- Hardware Security
- Embedded System & Board Test
- Test & Security of Quantum Circuits
- Test & Security of Photonic Circuits
- Test & Security of Emerging Memory Technologies
- Test & Security of Machine Learning Hardware
- Machine Learning for Test & Security
- Functional Debug through Scan
- Fault Modeling and Simulation
- Low-Power IC Test
- Microsystems/MEMS/Sensors Test
- Memory Test and Repair
- Test for 3D & Heterogeneous Integration
- Yield Optimization

Key Dates:

Regular paper abstract:

Nov. 13, 2026

Regular paper PDF:

Nov. 20, 2026

Regular paper notification:

Jan. 29, 2027

Late-breaking results submission:

Feb. 5, 2027

Late-breaking results notification:

Feb. 26, 2027

Submissions:

Scientific Papers: complete manuscripts - up to 6 pages in standard IEEE two-column format (references do not count towards the page limit).

Special Session and Innovative Practices Proposals: proposals may include presentations on hot topics, panels, and embedded tutorials. Every proposal must include a 150-to-200 word abstract - the name of the organizers and a list of at least three speakers with tentative presentation titles.

Late-breaking results (LBR): 3-page (including ref) standard IEEE two-column extended abstracts that should cover new research relevant to VTS research topics. Typical formats are (i) breakthrough approaches or ways to solve a known problem from a novel research angle, (ii) breakthrough results, where sufficient work has been accomplished to indicate the viability of the work.

Submit your papers at <https://welcome.molesystems.com/ttcc/VTS/2027>

The VTS review process is DOUBLE BLIND

Check out VTS
2027 website
ttcc-vts.org



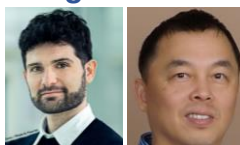
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