

# TEST RELIABILITY AND SECURITY CHALLENGES IN VLSI SYSTEMS

## CALL FOR PAPERS

The IEEE VLSI Test Symposium (VTS) explores emerging trends and novel concepts in test, reliability, calibration, validation, yield, and security of microelectronic circuits and systems. The VTS Program Committee invites original - unpublished paper submissions for VTS 2024 Proposals for the innovative practices and special sessions tracks are also invited.

For more information, visit the web site: [https://tttc-vts.org/public\\_html/new/2024/](https://tttc-vts.org/public_html/new/2024/)

### Major topics include but are not limited to:

Analog - Mixed-Signal - RF Test	Embedded System & Board Test	On-Line Test & Error Correction
ATPG & Compression	Radiation effects and testing	Power & Thermal Issues in Test
Silicon Debug	Emerging Technologies Test and Reliability	System-on-Chip (SOC) Test
Automotive Test & Safety	Fault Modeling and Simulation	Test & Reliability of Biomedical Devices
Built-In Self-Test (BIST)	Low-Power IC Test	Test & Reliability of High-Speed I/O
Defect & Current Based Test	Machine Learning in Test - Yield and Reliability	Test & Reliability of Machine Learning Systems
Defect & Fault Tolerance	Microsystems/MEMS/Sensors Test	Test Quality & Reliability
Delay & Performance Test	Memory Test and Repair	Test Standards & Economics
Design for Testability - Yield or Reliability	2.5D - 3D & SiP Test	Test Resource Partitioning
Pre-silicon Design Verification & Validation	Yield Optimization	Transient & Soft Errors
Post-silicon Validation		FPGA Test
Hardware Security		

### New hot topics:

This year VTS puts particular emphasis on enlarging its scope soliciting submissions on **silent data corruption, test, reliability and security of AI, fault models and reliability of in-memory computing hardware, test infrastructure for local production, and quantum computing.**

### Key Dates:

Paper registration:

**Oct. 9, 2023**

**Oct 20, 2023**

Paper PDF upload:

**Oct. 15, 2023**

**Oct 27, 2023**

Questions to authors:

**Dec. 9, 2023**

Submission of rebuttal:

**Dec. 14, 2023**

Notification:

**Dec. 23, 2023**

Camera-ready upload:

**Feb. 03, 2024**

### Submissions:

**Scientific Papers:** complete manuscripts - up to 6 pages in standard IEEE

two-column format (references do not count towards the page limit).

### Special Session and Innovative Practices Proposals:

Proposals may include presentations on hot topics - panels - embedded tutorials. Every proposal must include a 150-to-200 word abstract - the name of the organizers and a list of at least three speakers with a tentative presentation title. The VTS review process is DOUBLE BLIND with REBUTTAL.

### Submit your papers at:

<https://welcome.molesystems.com/tttc/VTS/2024>

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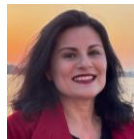
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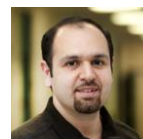
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