9th IEEE International Workshop on Testing Three-Dimensional Chiplets-based Stacked ICs

3D & Chiplet TEST

continuation of the popular 3D-TEST Workshop
in conjunction with IEEE International Test Conference / Test Week 2025
September 25-26, 2025
http://3dtest.tttc-events.org

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Yervant Zorian – Synopsys (US)

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Call for Submissions

The 3D & Chiplet TEST Workshop focuses exclusively on test and repair of chiplet-based stacked ICs, including 2.5D and 3D-Stacks based on hybrid bonding, through-silicon vias (TSVs), micro-bumps, and/or interposers. While these multi-die packages offer many attractive advantages, such heterogeneous integration, small form-factor, high bandwidth and performance, and low power dissipation, there are many challenges with respect to testing, monitoring and repairing such chiple based systems. The 3D & Chiplet TEST Workshop offers an ideal forum to present and discuss the challenges and emerging solutions among researchers and practitioners alike.

The 9th edition of 3D & Chiplet TEST will take place in conjunction with the IEEE International Test Conference (ITC) and is sponsored by the IEEE Philadelphia Section in concurrence with the Test Technology Technical Council (TTTC) of IEEE Computer Society

Topic Areas – You are invited to participate and submit your contributions to the 3D & Chiplet TEST Workshop. The areas of interest include (but are not limited to) the following topics:

- Defects due to Wafer Thinning
- DfT Architectures for 3D systems
- D2D PHY monitoring, test & repair
- EDA DfT Flow for 3D packages
- Lane Fault Models & Failure Analysis
- Fault-Tolerant Design for multi-die
- Handling and Testing Singulated stacks
- HBM base-die & stack test & repair
- Interposer Testing & Debugging
- Known-Good Die / Known-Good Stack
- Monitor interconnect signal integrity
- Pre-, Mid-, and Post-Bond Testing
- RAS for chiplet-based systems
- Stacking Yield, Redundancy & Repair
- Standards for 3D Test & Repair, P3405 1838
- Standards for test description 3dBlox
- Test Cost Modelling for 3D Packages
- Test Flow Optimization for 3D Packages
- Tester Architecture incl. ATE and BIST
- TSV-based lane test & repair
- UCie-based Multi-Die Test & Debug
- Wafer Probing and Probe Marks of 3D-SICs

Submission Instructions – Submissions must be sent as PDF files. The Workshop prefers Full Paper submissions (of up to six pages), but also allows Extended Abstract submissions (of at least two pages). Detailed submission instructions can be found at the Workshop's website: http://3dtest.tttc-events.org. All submissions will be evaluated for selection with respect to their suitability for the workshop, originality, technical soundness, and presented results.

Publications – 3D & Chiplet TEST focuses on early information sharing and free discussions; therefore, the workshop will not publish formal proceedings. Instead, the workshop will make available to all its registered participants an electronic workshop digest, which includes all material that authors/presenters are willing to contribute in PDF format: abstract, paper, slides, posters, background material, etc. This will allow authors to be free in their choice to submit their workshop paper later to a formal (IEEE or otherwise) journal, leveraging the audience feedback and discussions on the paper presentation at the 3D & Chiplet TEST Workshop.

Key Dates & Deadlines:
- Submission deadline : **June 27, 2025**
- Notification of acceptance : July **18, 2025**

Further Information

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