The 3D & Chiplet Test workshop Organizing Committee wants to thank his Sponsors and Supporters for their precious help

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3D & Chiplet Test Workshop - Preliminary Program

Thursday, November 7th

16:00 - 16:10 **OPENING –** Yervant Zorian (Synopsys – US), Saman Adham (TSMC) and Sreejit Chakrovarty (Ampere)

16:10 - 17:00 KEYNOTE: Chip-Act and 3D Integration, Rob Aitken *(NAPMP,US)*

17:00 - 18:30 SESSION 1: HBM Test Special Session

17:00 – 17:30 HBM Manufacturing Test Issues
→ Shu-Liang Nin (TSMC)
17:30 – 18:00 - New Silicon Health Challenges & opportunities with HBM4
→ Yervant Zorian (Synopsys)
18:00 – 18:30 Open Discussion on HBM Testing
→Open Microphone for workshop attendees

18:30 - 21:00 Workshop Reception

Friday, November 8th

8:00 - 9:00 SESSION 2: Chiplet Interconnect Repair

8:00 – 8:30 A Review of Interconnect Repair in HBM
→ Adrian Evans (CAE)
8:30 – 9:00 A Novel Chiplet Interconnect Repair Mechanism for Multi-Die System
→ Tapan Chakraborty

9:00 - 10:00 Embedded tutorial

TSMC 3DBlox standard
→ Sandeep Goel (TSMC)

10:00 – 10:30 Cofee Break

10:30 - 11:00 Keynote Speech

Test Challenges and Solutions for Fan-out Wafer-Level Packaging
→ Krishnendu Chakrabarty

11:00 - 12:00 Chiplet test Panel Session
Moderator: Sreejit Chakrovarty

12:00 – 13:00 Workshop Lunch

13:00 – 14:00 Chiplet Test in Data Centers

Chiplet Test Trends in Data Centers
→ Darshan Kubla and Pradipta (Microsoft)

14:00 – 16:00 Session 3

14:00 – 14:30 Scalable JTAG solution for 2.5D Multi-die Design è Ramu Setty (Marvell)

14:30 – 15:00 Testing Functional Interfaces And Complex PADs Within Multi-Die Packages With IEEE P3405
→ Anshuman Chandra (Siemens + ProteanTecs)

15:00 – 15:30 - MultiDie Physical aware DFT
→ Manish Arora (Synopsys)

15:300 – 16:00 Embedded HW structures to align test codebase in chiplet-based SoCs
→ David Akselord (AMD + McMaster University)

16:00 – 16:10 **CLOSING REMARKS**