CALL FOR PAPERS

The IEEE VLSI Test Symposium (VTS) explores emerging trends and novel concepts in testing, reliability and security of microelectronic circuits and systems. The VTS Program Committee invites original, unpublished paper submissions for VTS 2020. Proposals for the innovative practices and special sessions tracks are also invited.

Major topics include but are not limited to:

- Analog/Mixed-Signal/RF Test
- ATPG & Compression
- Silicon Debug
- Automotive Test & Safety
- Built-In Self-Test (BIST)
- Defect & Current Based Test
- Defect/Fault Tolerance
- Delay & Performance Test
- Design for Testability (DFT)
- Design Verification/Validation
- Embedded System & Board Test
- Embedded Test Methods
- Emerging Technologies Test
- FPGA Test
- Fault Modeling and Simulation
- Hardware Security
- Low-Power IC Test
- Microsystems/MEMS/Sensors Test
- Memory Test and Repair
- On-Line Test & Error Correction
- Power/Thermal Issues in Test
- System-on-Chip (SOC) Test
- Test Standards & Economics
- Test of Biomedical Devices
- Test of High-Speed I/O
- Test Quality and Reliability
- Test Resource Partitioning
- Transients and Soft Errors
- 2.5D, 3D and SiP Test
- Yield Optimization

VTS 2020 will present a Best Paper Award, a Best Special Session Award, and a Best Innovative Practices Session Award based on the evaluations of reviewers, attendees, and an invited panel of judges. We also plan to organize various Student Activities including the TTTC Best Doctoral Thesis Contest, details for which will be made available through the VTS website.

Submissions

6 pages in a standard IEEE two columns format.
Submit at: http://www.tttc-vts.org

KEY DATES

- Oct 4, 2019 - Title/Abstract Registration
- Oct 11, 2019 - Paper (PDF) upload
- Dec 10, 2019 - Notifications
- Feb 7, 2020 - Camera ready upload

For information, visit www.tttc-vts.org