Technical Program

36th IEEE VLSI TEST SYMPOSIUM (VTS 2018)

http://www.tttc-vts.org

IEEE Philadelphia Section

IEEE COMPUTER SOCIETY

Hyatt Centric Fisherman's Wharf
San Francisco, California, USA
April 22nd - April 25th, 2018

36th IEEE VLSI Test Symposium (VTS 2018)
San Francisco, California, USA, April 22 - 25, 2018

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Welcome Message

Welcome to VLSI Test Symposium (VTS) 2018, the thirty-sixth in a series of annual symposia that focuses on innovation in the field of testing of integrated circuits and systems.

The VTS 2018 program starts with a plenary keynote address from Philip Gadd, who is the Vice President of Data Center Group and General Manager Silion Photonics Product Division at Intel. He will share the challenges in design and test of silcon photonics and its applications in the Data Center Era. This will be followed by an invited keynote address from University of Iowa Foundation Distinguished Professor Reddy M. Sudhakar on "Test Drivers - Past, Present, and Future".

The core of VTS 2018, the three day technical program, responds to the many trends and challenges in the semiconductor design and manufacturing industries, with papers and presentations in the research paper sessions covering the core set of test topics: Analog, Mixed-Signal & RF Test; Delay and Performance Testing; ATPG & Test Compression; Design for Test, Debug and Reliability; Memory Testing and Repair; Reliability Analysis and Yield Optimization; Hardware Security; Test Economics and Test Standards; Test Quality and Reliability.

VTS also hosts the E.J. McCluskey Doctoral Thesis Competition to showcase the exciting student research in test. Following the new Student Activities Program instituted in 2017, VTS has another new student-focused initiative this year – PhD Student Forum– to encourage Ph.D. students to participate in the conference.

VTS continues its tradition of drawing the leading test practitioners and researchers in both industry and academia to contribute to the innovative practices (IP), special sessions, and new topic sessions, enabling it to be the venue where future technology trends and test challenges are deliberated, test practices are shared, and test research roadmap is chartered. This year, we have a rich offering of diverse topics in the IP and special sessions: Recent Developments in Hardware Security, Intelligent Sensor Nodes, how Machine Learning transform test, Reliability and Vulnerability of Neuromorphic Computing Systems, Silicon Photonics for Future Manycore Computing, Wireless Revolution in On-Chip Communication, impacts of Approximate Computing in Verification, Test and Reliability of Integrated Circuits, BIST/Calibration of A/MS devices, ISO26262 EDA, Test in Asia, Design & Test for Flexible Hybrid Electronics, Memory Test Practice, Functional Testing

and Fault Simulation for Functional Safety. A fact worth mentioning is two hot topics, machine learning and silicon phtonics, are offered in both IP and special sessions. One new topic session is offered with focus on Quantum Systems to study its challenges in design, test, and integration.

The popular Monday Evening Wine-and-Cheese Panel will discuss how new advances in Artificial and Machine Intelligence can impact jobs in Test and EDA.

Prior to the start of the conference program, two half-day tutorials will also be offered on Machine Learning and Its Applications in Test and Learning Techniques for Reliability Monitoring, Mitigation and Adaptation.

The social program at VTS provides an opportunity for informal technical discussions among participants. VTS 2008 attendees will experience the beauty, history and infamy of Alcatraz Island on San Francisco Bay and enjoy delectable local cuisine with a stunning San Francisco Bay view at Bristo Boudin.

VTS is the result of the work of many dedicated volunteers: the reviewers, the best paper award judges, the Program Committee, the Organizing Committee, and the Steering Committee. We wholeheartedly thank them all. We also wish to thank all the authors who submitted their work to VTS 2018, and the program participants for their contributions to the Symposium. We thank the IEEE Computer Society, the IEEE Philadelphia Section and the IEEE Computer Society Test Technology Technical Council (TTTC) for the continued technical sponsorship and support. Furthermore, we are indebted to ams AG, Dialog Semiconductor, and AdvanTest, the Premier Corporate Supporters for VTS 2018, as well as our Corporate Supporter, Mentor Graphics, for their partnership and continued support of this symposium.

We hope that you will find VTS 2018 enlightening, thought-provoking, rewarding, and enjoyable. We wish you all a fun-filled and productive week in the San Francisco area and we hope that you will keep making VTS a success by actively participating in it, assisting in its organization, and letting us always know how we can improve the symposium experience and increase its value for its audience.

Thank you all for coming!

General Chair
C.H. Chiang

Program Chairs
Amit Majumdar
Mehdi Tahoori

The VLSI Test Symposium is sponsored by the Test Technology Technical Council (TTTC) of the IEEE Computer Society

The IEEE promotes the engineering process of creating, developing, integrating, sharing, and applying knowledge about electronic and information technologies and sciences for the benefit of humanity and the profession

IEEE
Philadelphia Section

The purposes of this IEEE Society shall be scientific, literary, and educational in character. The Society shall strive to advance the theory, practice, and application of computer and information processing science and technology and shall maintain a high professional standing among its members. The scope of the Society shall encompass all aspects of theory, design, practice, and application relating to computer and information processing science and technology

IEEE COMPUTER SOCIETY

TTTC's goals are to contribute to our members' professional development and advancement, to help them solve engineering problems in electronic test, and to help advance the state of the art. In particular, TTTC aims at facilitating the knowledge flow in an integrated manner, to ensure overall quality in terms of technical excellence, fairness, openness, and equal opportunities

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REGISTRATION

The IEEE VLSI Test Symposium explores emerging trends and novel concepts in the testing of integrated circuits and systems. The symposium is a leading international forum where many of the world's leading test experts and professionals from both industry and academia join to present and debate key issues in testing. VTS 2018 addresses key trends and challenges in the semiconductor design and manufacturing industries through an exciting program that includes Keynote and Plenary Talks, Technical Paper Sessions, Embedded Tutorials, Panels, Hot Topic Sessions, Half-day Tutorials, the Innovative Practices Track, and all Students activities.

SYMPOSIUM REGISTRATION

Full registration *includes breakfasts, lunches, coffee breaks, social event, and electronic distribution of the symposium proceedings.*
Student registration *includes all of the above except the social event.*

Discounted advance registration prices are valid until 04/13/18. Cancellations are allowed until 04/13/18 at an administrative fee of $75. Substitutions are allowed until 04/15/18, at no cost. For either of the above or any other registration questions, please contact the registration chair, Chintan Patel.

VTS 2018 April 22 - 25	Advance Rate (April 13, 2018, midnight PDT)	Onsite Rate (After April 13, 2018)
IEEE Member Registration (Member rates are available only to current members of IEEE. Please enter your valid membership number in order to qualify!)	$650.00	$770.00
IEEE Lifetime Member Registration	$350.00	$425.00
IEEE Non-Member Registration	$795.00	$925.00
IEEE Student Member Registration (Valid student ID may be required at onsite registration check-in.)	$350.00	$425.00
Student IEEE Non-Member Registration (Valid student ID may be required at onsite registration check-in.)	$500.00	$600.00
Social Event and Dinner Ticket (One Ticket is included for those paying IEEE Member or Non-Member VTS rates). Students and companions of registered attendees may select to purchase a social ticket at the end of the registration process.	$125.00	$125.00
Additional Lunch Ticket (Lunch is included for those paying IEEE/CS Member or Non-Member VTS rates). Companions of registered attendees may select to purchase lunch tickets at the end of the registration process.	$65 per day	$65 per day

TTEP Tutorials Registration

April 22nd, 8:30 a.m. - 04:30 p.m.

	Advance Rate (April 10, 2018, midnight PDT)	Onsite Rate (After April 10, 2018)
Single Tutorial (morning or afternoon) April 22		
IEEE Member, Student or Lifetime Member	$200.00	$270.00
IEEE Non-Member	$240.00	$330.00
Two Tutorials (morning and afternoon) April 22		
IEEE Member, Student or Lifetime Member	$300.00	$350.00
IEEE Non-Member	$360.00	$420.00

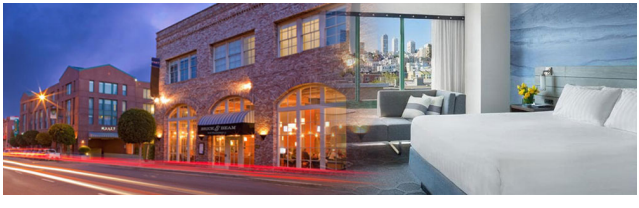
San Francisco is the cultural, commercial, and financial center of Northern California. A popular tourist destination, San Francisco is known for its cool summers, fog, steep rolling hills, eclectic mix of architecture, and landmarks, including the Golden Gate Bridge, cable cars, the former Alcatraz Federal Penitentiary, Chinatown district and Fisherman's Wharf where VTS2018 hotel, Hyatt Centric Fisherman's Wharf, is located.

San Francisco International Airport (IATA: SFO) is a major international gateway to Asia and Europe. Located across the bay, Oakland International Airport (IATA: OAK) is a popular, low-cost alternative to SFO. Bay Area Rapid Transit (BART), is a rapid transit public transportation system serving the San Francisco Bay Area. The San Francisco Municipal Railway (MUNI) is the public transit system for the city and county of San Francisco, California.

Detail instructions of public tranportation system to Fisherman's Warf can be found at ***http://www.fishermanswharf.org/public-transportation.html***. Uber, Lyft and taxi are always covenient to take you around in San Francisco.

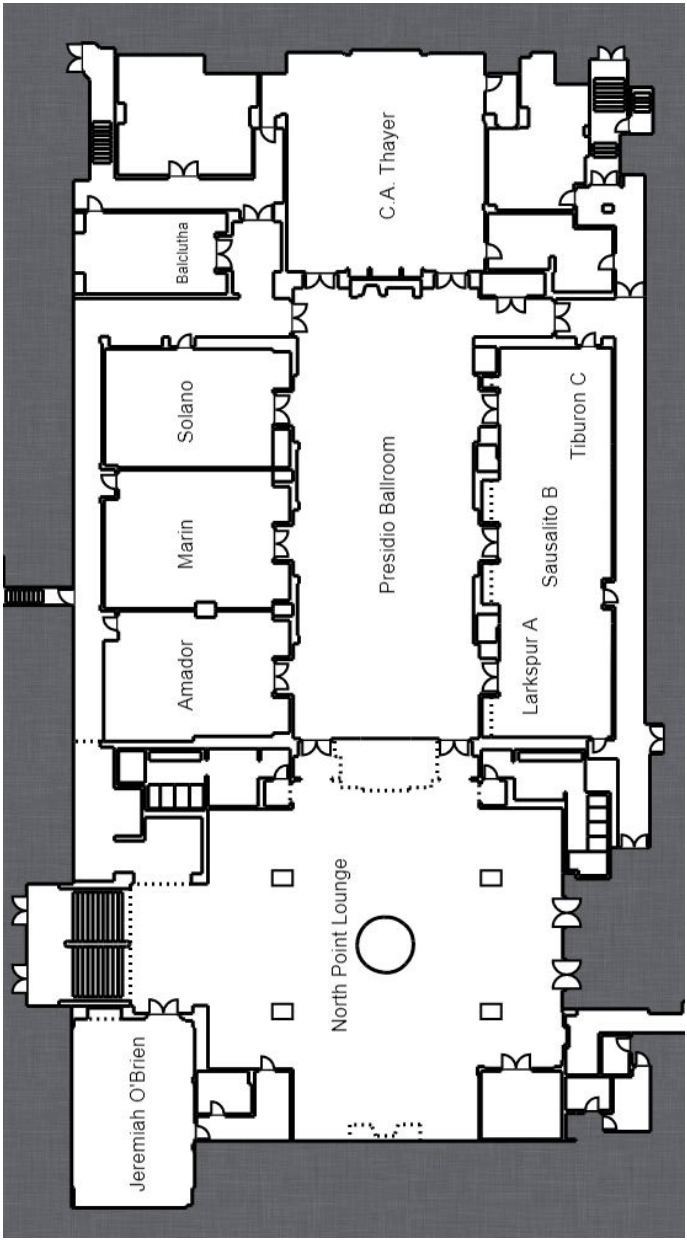
The 36th IEEE VLSI Test Symposium will be held at Hyatt Centric Fisherman's Wharf. It is a centrally located San Francisco hotel near top attractions including Lombard Street, Pier 39, Golden Gate Bridge, and the historic network of cable cars. It's the perfect Fisherman's Wharf hotel for exploring attractions in the city offering everything you need for a great stay and wonderful hotel experience in San Francisco.

Hotel Reservation Procedure:
Discounted rates of $199 for single/double room is made available to VTS'18 attendees until March 30, 2018 at 5pm PDT or until the room block is sold out, whichever comes first. The proce is exclusive of applicable sales/room tax, currently 14% percent, 2.25% San Francisco Improvement District Assessment Fee and 0.195% California Tourism Assessment Fee. Housekeeping and other gratuities will be at guest discretion.



Visit the following web-site to reserve a room:
https://aws.passkey.com/go/IEEEVTS2018

Hotel Home Page: ***http://www.fishermanswharf.centric.hyatt.com***
Address: 555 North Point Street, San Francisco, California, USA, 94133
Telephone: +1 (415) 563-1234


Balclutha
C.A. Thayer
Solano
Marin
Amador
Presidio Ballroom
Larkspur A
Sausalito B
Tiburon C
North Point Lounge
Jeremiah O'Brien

VTS'18 is offering 2 half-day TTEP tutorials, one in the morning and one in the afternoon, for which a separate registration fee is required. Attendees who register for the tutorials may select either one or both of the offerings.

All tutorials qualify for credit towards IEEE TTTC certification under the TTEP program. Attendees of tutorials receive study material, handouts, breakfast and coffee breaks. The study material includes copies of the presentation and bibliographical material, and, when applicable, a relevant textbook (textbooks are provided to attendees who register at IEEE/CS member or non-member rates).

Morning Tutorial (8:30 a.m. – 12:00 p.m.)

Tutorial #1: Machine Learning and Its Applications in Test

Presenter: *Yu Huang and Gaurav Vega (Mentor, A Siemens Business)*
Room: *TBA*

In this tutorial, we will start by covering the basics of machine learning. We will proceed to give a brief overview of the new and exciting field of deep learning. We will show how easy it is to try using machine learning and deep learning, thanks to powerful, free libraries. After offering the required background in machine learning, we will review several important papers in the field of DFT, diagnosis, yield learning, and root cause analysis, which use machine learning algorithms for solving various problems. Finally, we will propose future research directions in the area of testing, where we think machine learning (especially deep learning) can make a big impact.

Afternoon Tutorial (1:00 p.m. – 4:30 p.m.)

Tutorial #2: Learning Techniques for Reliability Monitoring, Mitigation and Adaptation

Presenter: *Mehdi Tahoori (Karlsruhe Institute of Technology)*
Room: *TBA*

With increasing the complexity of digital systems and the use of advanced nanoscale technology nodes, various process and runtime variabilities threaten the correct operation of these systems. The interdependence of

these reliability detractors and their dependencies to circuit structure as well as running workloads makes it very hard to derive simple deterministic models to analyze and target them. As a result, machine learning techniques can be used to extract useful information which can be used to effectively monitor and improve the reliability of digital systems. These learning schemes are typically performed offline on large data sets in order to obtain various regression models which then are used during runtime operation to predict the health of the system and guide appropriate adaptation and countermeasure schemes.

Registration: North Point Lounge
Lunch & Breaks: North Point Lounge
VTS Office: Balclutha
Room for Fringe Meetings: Balclutha
Speaker Room: Training Room

Monday, April 23, 2018

07:30AM - 08:30AM	Registration and Breakfast
08:30AM - 10:30AM	**Plenary Session** HALL : Presidio Ballroom **Welcome Message:** **Program Introduction:** **Opening Keynote: High volume manufacturing and test of high-speed silicon photonics devices for next generation data center deployments.** *Philip Gadd, Vice President of Data Center Group & General Manager of Silicon Photonics Product Division (Intel)* **Invited Keynote: Test Drivers - Past, Present, and Future** **Speaker:** *Sudhakar M. Reddy, U. of Iowa Foundation, Distinguished Professor, Electrical and Computer Engineering Dept., U. of Iowa*
10:30AM - 11:00AM	Break
11:00AM - 12:00PM	**Sessions 1**

Session 1A: Analog Test
HALL : Banquet ABC

Moderator: Stephen Sunter *(Mentor, A Siemens Business)*

- **Group Delay Measurement of Frequency Down-Converter Devices Using Chirped RF Modulated Signal** *Pete Sarson (ams AG), Yanagida Tomonori, Kosuke Machida (Gunma U.)*
- **A Coherent Subsampling Test System Arrangement Suitable for Phase Domain Measurements** *Young Gouk Cho (Ciena), Gordon Roberts (McGill U.), Sadok Aouini, Mahdi Parvizi, Naim Ben-Hamida (Ciena)*
- **An Oscillation-Based Test technique for on-chip testing of mm-wave phase shifters** *Marc Margalef-Rovira, Manuel Barragan, Philippe*

Ferrari (TIMA Laboratory), E. Sharma, Emmanuel Pistono, S. Bourdel (IMEP-LaCH)

Session 1B: Hot Topic: Recent Developments in Hardware Security
HALL : CA Thayer

Organizer & Moderator: Jeyavijayan Rajendran *(Texas A&M U.)*

- **A path toward early adoption of lattice-based cryptography schemes in hardware** *Ro Commarota (Qualcomm Inc.)*
- **Device Aging and Power Analysis Attacks** *Naghmeh Karimi (U. of Maryland Baltimore County)*
- **Backdoored Neural Networks (BadNets): A New Challenge for the Test Community** *Siddharth Garg (New York U.)*

IP Session 1C: Memory Test Practice
HALL : Presidio Ballroom

Organizer & Moderator: *Ramesh Tekumalla (Broadcom Inc.)*

- **Leveraging Embedded Memory Test and Repair for Functional Safety** *M. Casarsa (ST Microelectronics) Gurgen Harutyunyan (Synopsys)*
- **Memory Test Capabilities for Addressing Test Cost Reduction and Functional Safety Needs** *Kaitlyn Chen and Ramesh Sharma (Intel Corporation) Giri Pondichetty and Martin Keim (Mentor Graphics)*
- **Improving Array BIST for Infield Test and Repair and Yield Analysis** *Sreejit Chakravarty (Intel Corporation)*

12:30PM - 01:30PM	**Lunch break**

01:30PM - 02:30PM

Sessions 2

Session 2A: Hardware Security

HALL : Banquet ABC

Moderator: *Adit Singh (Auburn U.)*

- **ATPG-Based Cost-Effective, Secure Logic Locking** *Abhrajit Sengupta (New York U.), Mohammed Nabeel (New York U. Abu Dhabi), Muhammad Yasin (New York U.), Ozgur Sinanoglu (New York U. Abu Dhabi)*
- **Modeling and Test Generation for Combinational Hardware Trojans** *Ziqi Zhou, Ujjwal Guin, Vishwani Agrawal (Auburn U.)*
- **Modeling Attacks on Strong Physical Unclonable Functions Strengthened by Random Number and Weak PUF** *Jing Ye, Yu Hu(State Key Laboratory of Computer Architecture, Institute of Computing Technology, Chinese Academy of Sciences), Qingli Guo, Xiaowei Li, Huawei Li (Institute of Computing Technology, Chinese Academy of Sciences)*

Session 2B: Hot Topic: Approximate Computing

HALL : CA Thayer

Organizers & Moderators: *Alberto Bosio (LIRMM) & Stefano Di Carlo (Politecnico di Torino)*

- **Formal verification techniques for search-based functional approximation of digital circuits** *Lukas Sekanina & Zdenek Vasicek (FIT)*
- **Testing Approximate Digital Circuits** *Alberto Bosio & Marcello Traiola (LIRMM)*
- **Benefits and Challenges of Approximate Computing in Applications Reliability** *Paolo Rech, Daniel Oliveria & Fernando Fernandes, (UFRGS)*

IP Session 2C: Quality Levels of A/MS Devices
HALL : Presidio Ballroom

Organizer & Moderator: *Peter Sarson (Dialog Semiconductor)*

- **Producing defect-free IC's by combining electrical test data and silicon Inspection data** *Wim Dobbelaere (OnSemiconductor)*
- **Using fault injection to determine ASIL level** *Massimo Violante (Politecnico di Torino)*
- **IEEE P2427: Proposing the essential framework for measuring defect coverage in analog circuits** *Jeff Rearick (AMD)*

02:30PM - 03:00PM | Break

03:00PM - 04:00PM | **Sessions 3**

Session 3A: Memory
HALL : Banquet ABC

Moderator: *Martin Keim (Mentor, A Siemens Business)*

- **Hardware Trojan Attacks in Embedded Memory** *Tamzidul Hoque, Robert Karam, Swarup Bhunia (U. of Florida), Xinmu Wang, Abhishek Basak (Case Western Reserve U.)*
- **High efficient low cost EEPROM screening method in combination with an area optimized byte replacement strategy which enables high reliability EEPROMs** *Gregor Schatzberger, Friedrich Leisenberger, Pete Sarson, Andreas Wiesner (ams AG)*
- **Test Challenges and Solutions for Emerging Non-Volatile Memories** *Mohammad Nasim Imtiaz Khan, Swaroop Ghosh (Pennsylvania State U.)*

Session 3B: Hot Topic: Neuromorphic Computing
HALL : CA Thayer

Organizer & Moderator: *Yiran Chen (Duke U.)*

- **Reliability Effects of Resistive Synaptic Devices on Neuromorphic Computing System Performance** *Shimeng Yu (Arizona State U.)*
- **Reliability Analysis and Enhancement of the ReRAM based Neuromorphic Systems** *Chenchen Liu (Clarkson U.)*
- **Exploiting Deep Learning System-level Vulnerabilities from the Intelligent Supply Chain** *Wujie Wen (Florida International U.)*

IP Session 3C: ISO26262 EDA
HALL : Presidio Ballroom

Organizer: *Peter Sarson (Dialog Semiconductor)*
Moderator: *Wim Dobbelaere (OnSemiconductor)*

- **Analog Fault Simulation and Fault Injection** *Yervant Zorian (Synopsis)*
- **Measuring ISO 26262 Metrics and Fault Coverage Simultaneously for A/MS Circuits** *Stephen Sunter (Mentor, A Siemens Business)*

04:00PM - 04:30PM	Wine and Cheese
04:30PM - 06:00PM	**PLENARY EVENING PANEL:** Are we about to automate ourselves out of our jobs?
	HALL : Presidio Ballroom
	Moderator: *Stefano Di Carlo (Politecnico di Torino)*
06:30PM - 08:30PM	**PC Meeting (by invitation only)**
	HALL : Jeremiah O'Brien Room

Tuesday, April 24, 2018

07:30AM - 08:30AM	Registration and Breakfast
08:30AM - 09:30AM	**Sessions 4**

Session 4A: BIST
HALL : Banquet ABC

Moderator: *Jennifer Dworak (Southern Methodist U.)*

- **An Inter-Layer Interconnect BIST Solution for Monolithic 3D ICs** *Abhishek Koneru, Krishnendu Chakrabarty (Duke U.)*
- **A Built-In Self-Test Technique for Transmitter-Only Systems** *Maryam Shafiee, Jennifer Kitchen, Sule Ozev (Arizona State U.)*
- **Exploiting Built-In Delay Lines for Applying Launch-on-Capture At-Speed Testing on Self-Timed Circuits** *Omar Al-Terkawi Hasib (Ecole polytechnique of Montreal), Daniel Crepeau, Thomas Awad (Octasic), Andrei Dulipovici (E. Tech. Sup. Montreal), Yvon Savaria (Ecole Polytechnique Montreal), Claude Thibeault (E. Tech. Sup. Montreal)*

Session 4B: Hot Topic: Bringing Cores Closer Together: The Wireless Revolution in On-Chip Communication
HALL : CA Thayer

Organizer: *Partha Pratim Pande (Washington State U.)*
Moderator: *Sudeep Pasricha (Colorado State U.)*

- **Surfing on the Chip: Wired and Surface-Wave Integration for Network-on-Chip Architectures** *Terrence Mak (U. of Southampton)*
- **A Building Block 3D System with Inductive-Coupling Through Chip Interfaces** *Hiroki Matsutani (Keio U.)*
- **Designing Energy Efficient and Reliable Manycore Chip Enabled by Millimeter-Wave Wireless Links** *Partha Pratim Pande (Washington State U.)*

IP Session 4C: Fault Simulation for Functional Safety
HALL : Presidio Ballroom

Organizer: *Prashant Goteti (Intel)*
Moderator: *Sreejit Chakravarty (Intel)*

- **Accelerating Fault Injection and Diagnostic Coverage for FuSa** *Animesh Mishra (Intel)*
- **Functional Random Testing on the ATE targeting CPU SoC for Automotive Grade Products** *John M .Van Gelder (Xilinx)*
- **Fault Simulation and Modeling for Analog Test** *Mayukh Bhattacharya (Synopsys)*

09:30AM - 09:45AM | Break

09:45AM - 10:45AM | **Sessions 5**

Session 5A: Test Standards
HALL : Banquet ABC

Moderator: *Claude Thibeault (E. Tech. Sup. Montreal)*

- **Broadcast-Based Minimization of the Overall Access Time for the IEEE 1687 Network** *Zhanwei Zhong, Krishnendu Chakrabarty (Duke U.), Guoliang Li, Qinfu Yang, Jun Qian (Advanced Micro Devices)*
- **Efficient Parallel Testing: A Configurable and Scalable Broadcast Network Design Using IJTAG** *Saurabh Gupta, Jennifer Dworak (Southern Methodist U.), Jae Wu (Nvidia Graphics)*
- **Securing IJTAG Against Data-Integrity Attacks** *Rana Elnaggar, Krishnendu Chakrabarty (Duke U.), Ramesh Karri (NYU)*

Session 5B Hot Topic: Overcoming Reliability and Energy-Efficiency Challenges with Silicon Photonics for Future Manycore Computing
HALL : CA Thayer

Organizer: *Sudeep Pasricha (Colorado State U.)*
Moderator: *Partha Pratim Pande (Washington State U.)*

- **Exploring Power and Data Signaling Enhancements for Emerging Silicon Photonic Networks-on-Chip** *Sudeep Pasricha (Colorado State U.)*
- **Toward a Cross-Layer Synthesis Methodology for Wavelength-Routed Optical Networks-on-Chip** *Davide Bertozzi (U. of Ferrara)*
- **Thermal-Aware Design Methods in Optical Networks-on-Chip** *Hui Li (Xidian U.)*

IP Session 5C: Innovative Test Practices in Japan
HALL : Presidio Ballroom

Organizer & Moderator: *Kazumi Hatayama (Gunma U.)*

- **Analysis and Evaluation Method of Complex Analog Filter** *Koji Asami (Advantest, Japan)*
- **A DFT based approach to functional safety for automotive MCU** *Jun Matsushima and Yoichi Maeda (Renesas Electronics, Japan)*

10:45AM - 11:00AM Break

11:00AM - 12:00PM **Sessions 6**

Session 6A: ATPG
HALL : Banquet ABC

Moderator: *Alex Orailoglu (UCSD)*

- **Efficient Generation of Parametric Test Vectors for AMS chips with an Interval Constraint Solver** *Felix Neubauer, Jan Burchard, Pascal Raiola, Bernd Becker, Matthias Sauer (U. of Freiburg), Jochen Rivoir (Advantest)*
- **Enhanced Hotspot Detection Through Synthetic Pattern Generation and Design of Experiments** *Gaurav Rajavendra Reddy, Constantinos Xanthopoulos (U. of Texas at Dallas), Yiorgos Makris (UT Dallas)*

- **Staggered ATPG with Capture-per-Cycle Observation Test Points** *Jerzy Tyszer (Poznan U. of Technology), Yingdi Liu, Sudhakar Reddy (U. of Iowa), Janusz Rajski (Mentor Graphics Corporation), Jedrzej Solecki (Mentor – A Siemens Business)*

Session 6B: Hot Topic: Intelligent Sensor Nodes

HALL : CA Thayer

Organizers & Moderators: *Kanad Basu (NYU) & Shreyas Sen (Purdue U.)*

- **The Challenge of Large-Scale Connectivity: Design, Validation, and Debug** *Sandip Ray (U. of Florida)*
- **Hierarchical Checking and Adaptation Strategies for Robust Intelligent Autonomous Systems** *Abhijit Chatterjee (Georgia Institute of Technology)*
- **Solving the Drift Problem of Biological and Chemical Sensors in the Field** *Sule Ozev and Jennifer Blain Christen (Arizona State U.)*
- **Analog, Mixed-Signal and MEMS DFT and its Use for Intelligent Sensors** *Salvador Mir (U. Grenoble Alpes, CNRS, TIMA)*

IP Session 6C: Silicon Photonics

HALL : Presidio Ballroom

Organizer & Moderator: *Eugene Atwood (IBM)*

- **The status, needs and potential solutions related to testing photonic devices and products including those that Incorporate Photonic Integrated Circuits (PIC)** *Dick Otte (PROMEX)*
- **Challenges and Opportunities in Integrated CMOS/Photonics Test** *Roy Meade (Ayer Lab)*
- **Machine Learning Application For Silicon Photonics Transceiver Testing** *Woosung Kim (Intel Corporation)*

12:10PM - 01:10PM	Lunch
01:10PM - 02:10PM	**Panel Discussion 1:** Solutions to Automotive Test Challenges: Are we there yet? HALL : Banquet ABC **Moderator:** *Paolo Bernardi(Poli. Torino)* **Panelists:** Davide Appello*(ST)* Jon Colburn *(Nvidia)* Gustavo Espinosa *(Intel)* Nir Maor *(Qualcomm)* Yervant Zorian *(Synopsys)*
	Panel Discussion 2: Challenges for Heterogeneous Integration: Learning from Past Experiences to Solve Problems of the Future HALL : CA Thayer **Moderator:** *Sule Ozev (ASU)* **Panelists:** Jennifer Kitchen *(ASU)* Krish Chakrabarty *(Duke U.)* Nui Chong *(Xilinx)*
	Student Poster Presentations HALL : Presidio Ballroom **Organizers:** *Naghmeh Karimi, (U. of Maryland Baltimore County - USA)*
02:10PM - 02:30PM	Break
02:30PM - 09:00PM	**Social Event**

Wednesday, April 25, 2018

07:30AM - 08:30AM	Registration and Breakfast
08:30AM - 09:30AM	**Sessions 7**

Session 7A: Reliability
HALL : Banquet ABC

Moderator : *Yiorgos Makris (UT Dallas)*

- **Systematic b-Adjacent Symbol Error Correcting Reed-Solomon Codes with Parallel Decoding** *Abhishek Das, Nur Touba (U. of Texas at Austin)*
- **Circuit-Level Reliability Simulator for Front-End-of-Line and Middle-of-Line Time-Dependent Dielectric Breakdown in FinFET Technology** *Kexin Yang, Rui Zhang, Linda Milor (Georgia Institute of Technology), Taizhi Liu (Georgia Tech)*
- **On-Line Monitoring and Error Correction in Sensor Interface Circuits Using Digital Calibration Techniques** *Sascha Heinssen, Theodor Hillebrand, Maike Taddiken, Steffen Paul, Dagmar Peters-drolshagen (U. of Bremen)*

Session 7B: Hot Topic: BIST/Calibration of A/MS devices
HALL : CA Thayer

Organizer & Moderator: *Peter Sarson (Dialog Semiconductor)*

- **Trimming: The Challenge for Yield and Test Cost** *Hans Martin von Staudt (Dialog Semicondutor)*
- **High accuracy trim, calibration and testing of integrated on-chip op-amps** *James Izon (Texas Instruments)*
- **Dynamic Testing and Trimming for Embedded DC-DC Converters** *Sule Ozev (Arizona State U.)*

IP Session 7C: Machine Learning for Emerging Applications
HALL : Presidio Ballroom

Organizer & Moderator: Yu Huang (Mentor, A Siemens Business)

- **Overcoming the Challenges of Hotspot Detection using Deep Learning** *Kareem Madkour (Mentor, A Siemens Business)*
- **Data-Driven Health Monitoring Solution for Network Devices** *Zhaobo Zhang (Huawei Technologies Co. Ltd)*
- **Data Collection of a Trojan Insertion Hardware Emulator for Machine Learning** *Alfred L. Crouch, Peter L. Levin & Eve Hunter (Amida Technology Solutions, Inc.)*

09:30AM - 09:50AM — Break

09:50AM - 10:50AM — **Sessions 8**

Session 8A: Machine Learning in Test
HALL : Banquet ABC

Moderator : *Haralampos Stratigopoulos (Sorbonne U., CNRS, LIP6)*

- **IC Layout Weak Point Effectiveness Evaluation based on Statistical Methods** *Fang Lin, Ke Huang (San Diego State U.), Ali Ahmadi, Kannan Sekar, Pan Yan (Global Foundries)*
- **Analyzing and Mitigating the Impact of Permanent Faults on a Systolic Array Based Neural Network Accelerator** *Jeff Zhang, Tianyu Gu, Kanad Basu, Siddharth Garg (New York U.)*
- **IR Drop Prediction of ECO-Revised Circuits Using Machine Learning** *Shih-Yao Lin, Yen-Chun Fang, Yu-Ching Li, Yu-Cheng Liu, Chien-Mo Li, Tsung-Shan Yang, Shang-Chien Ling (National Taiwan U.), Eric Jia-Wei Fang (MediaTek Inc.)*

Session 8B: Hot Topic: Machine Learning for Test and Diagnosis
HALL : CA Thayer

Organizer : *Yu Huang (Mentor, A Siemens Business)*
Moderator : *Arani Sinha (Intel Corporation)*

- **Data-Driven Resiliency Solutions for Boards and Systems** *Krishnendu Chakrabarty (Duke U.)*
- **Machine Learning For Feature-Based Analytics in Some Test Applications** *Li-C. Wang (UCSB)*
- **Supervised Techniques for Volume Diagnosis** *Gaurav Veda (Mentor, A Siemens Business)*

IP Session 8C: Challenges, Opportunities and Solutions to Hardware Security
HALL : Presidio Ballroom

Organizer & Moderator: *Huawei Li (CAS)*

- **Is EDA Industry Ready for Design for Security and Security Validation Challenges?** *Sohrab Aftabjahani (Intel)*
- **Enabling Full SoC Hardware/Software Security Verification** *Jason Oberg (Tortuga Logic)*
- **Finding Opportunities to Apply Hardware Security** *Michael Chen, Mentor (A Siemens Business)*

10:50AM - 11:10AM — Break

11:10AM - 12:40PM — **Sessions 9**

Session 9A: Test Data Analysis
HALL : Banquet ABC

Moderator : *Janusz Rajski (Mentor Graphics Corp.)*

- **Fast Fault Coverage Estimation of Sequential Tests Using Entropy Measurements** *Sarmad Tanwir, Michael Hsiao (Virginia Tech)*
- **Real-Time Monitoring of Test Fallout Data to Quickly Identify Tester and Yield Issues in a Multi-Site Environment** *Qutaiba Khasawneh (Oncor), Jennifer Dworak, Ping Gui, Benjamin Williams, Alan Elliott (SMU), Anand Muthaiah (Tessolve)*
- **Online Information Utility Assessment for Per-Device Adaptive Test Flow** *Yanjun Li (U. of*

Electronic Science and Technology of China), Ender Yilmaz (NXP Semiconductors), Pete Sarson (ams AG), Sule Ozev (Arizona State U.)

Session 9B New Topic: Quantum Systems: Next Challenges in Design, Test, Integration
HALL : CA Thayer

Organizers & Moderators: *Bozena Kaminska (Simon Fraser U.) & Bernard Courtois (BC Consulting)*

- **Challenges and opportunities of Si-based Quantum bits integration** *Carlo Reita (CEA-LETI)*
- **Challenges in scaling up silicon-based quantum processors** *Jonathan Baugh (U. of Waterloo)*
- **Building a supercomputing quantum processor at scale** *Gabriel Poulin-Lamarre (D-Wave Systems)*

Session 9C: TTTC 's E. J. McCluskey Doctoral Thesis Award
HALL : Presidio Ballroom

Organizer: *Naghmeh Karimi (U. of Maryland Baltimore County)*

12:40PM - 02:00PM — Lunch

02:00PM - 03:00PM — **Sessions 10**

Session 10A: Reliability, Security, Diagnosis
HALL : Banquet ABC

Moderator: *Tapan Chakraborty (Qualcomm Inc.)*

- **NOIDA: Noise-resistant Intra-cell diagnosis** *Soumya Mittal, Ronald Blanton (Carnegie Mellon U.)*
- **Multi-faceted Microarchitecture Level Reliability Characterization for NVIDIA and AMD GPUs** *Alessandro Vallero, Stefano Di Carlo (Politecnico di Torino), Sotiris Tselonis, Dimitris Gizopoulos (U. of Athens)*
- **RF Circuit Authentication for Detection of Process Trojans** *Fatih Karabacak, Kitchen Jennifer, Sule Ozev (Arizona State U.), Richard Welker (Alphacore Inc.), Matthew Casto (Air*

Force Research Lab, Wright-Patterson Air Force Base)

Session 10B Hot Topic: Machine Learning and Big Data in Test
HALL : CA Thayer

Organizer & Moderator: *Marc Hutner (Teradyne)*

- **Machine Learning in Semiconductor Test: Can Deep Learning Save The Day?** *Yiorgos Makris (UT Dallas)*
- **Small Signals Extraction in Semiconductor Test & Manufacturing: Role of Machine Learning** *Amit Nahar (Texas Instruments)*
- **Adaptive Test: Machine Learning in Real Time on Big Data** *Haralampos-G. Stratigopoulos (Sorbonne U., CNRS, LIP6)*

IP Session 10C: Design & Test fo Flexible Hybrid Electronics
HALL : Presidio Ballroom

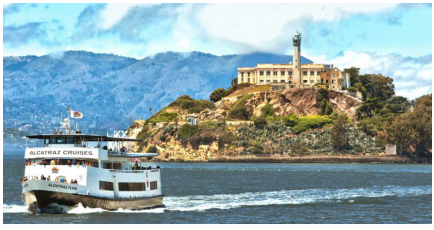
Organizer: *Jim Huang (Hewlett Packard Labs)*
Moderator: *Mango Chia-Tso Chao (NCTU)*

- **Process Design Kit (PDK) for Design and Test Challenges of Flexible Hybrid Electronics** *Jim Huang (HPE)*
- **Considerations for Design and Test of Flexible Hybrid Electronic Systems** *Jason Marsh (NextFlex)*
- **Design and Test Considerations for Flexible Hybrid Electronics Fabricated with High-Performance COTS ICs using RTI CircuitFilmTM Technology** *(Scott H. Goodwin, Micross Components)*

Session 10D: Town-Hall Meeting for NSF Student Program Participants
HALL : TBC

Moderator: *Naghmeh Karimi (U. of Maryland Baltimore County)*

This year our social event will start with a short (0.7 mile) walk from the conference venue to Pier 33 Alcatraz Landing, where we will board the cruise to Alcatraz Island in three groups.



All Alcatraz Island tour tickets include round-trip transportation, as well as the award-winning Cellhouse audio tour, available in Dutch, English, French, German, Italian, Japanese, Korean, Mandarin, Portuguese, Russian, and Spanish.

Upon the return from Alcatraz Island tour, another 0.6 mile walk from Pier 33 to Bistro Boudin, 160 Jefferson St, San Francisco, CA 94133, where we will continue to make connection with our VTS colleagues in the unique waterfront restaurant with legendary sourdough bread.

Precise instructions and directions will be distributed at the symposium.

36th IEEE VLSI TEST SYMPOSIUM - PROGRAM AT A GLANCE

MONDAY, APRIL 23, 2018			
07:30am - 08:30am	**REGISTRATION & BREAKFAST**		
08:30am - 10:30am	**PLENARY SESSION**		
11:00am - 12:00pm	**SESSION 1A:** Analog Test	**SESSION 1B:** Hot Topic: Recent Developments in Hardware Security	**IP SESSION 1C:** Memory Test Practice
12:30pm - 01:30pm	LUNCH		
01:30pm - 02:30pm	**SESSION 2A:** Hardware Security	**SESSION 2B:** Hot Topic: Approximate Computing	**IP SESSION 2C:** Quality Levels of A/MS Devices
03:00pm - 04:00pm	**SESSION 3A:** Memory	**SESSION 3B:** Hot Topic: Neuromorphic Computing	**IP SESSION 3C:** ISO26262 EDA
04:30pm - 06:00pm	**PLENARY EVENING PANEL**		

TUESDAY, APRIL 24, 2018			
07:30am - 08:30am	**REGISTRATION & BREAKFAST**		
08:30am - 09:30am	**SESSION 4A:** BIST	**SESSION 4B:** Hot Topic:Bringing Cores Closer Together: The Wireless Revolution in On-Chip Communication	**IP SESSION 4C:** Fault Simulation for Functional Safety
09:45am - 10:45am	**SESSION 5A:** Test Standards	**SESSION 5B:** Hot Topic: Overcoming Reliability and Energy-Efficiency Challenges with Silicon Photonics for Future Manycore Computing	**IP SESSION 5C:** Innovative Practices on Test in Japan
11:00am - 12:00pm	**SESSION 6A:** ATPG	**SESSION 6B:** Hot Topic: Intelligent Sensor Nodes	**IP SESSION 6C:** Silicon Photonics

36th IEEE VLSI TEST SYMPOSIUM - PROGRAM AT A GLANCE

12:10pm - 01:10pm	LUNCH		
01:10pm - 02:10pm	**PANEL DISCUSSION**	**POSTER SESSION**	
02:30pm - 09:00pm	SOCIAL PROGRAM		

WEDNESDAY, APRIL 25, 2018			
07:30am - 08:30am	**REGISTRATION & BREAKFAST**		
08:30am - 09:30am	**SESSION 7A:** Reliability	**SESSION 7B:** Hot Topic: BIST/Calibration of A/MS devices	**IP SESSION 7C:** Machine Learning for Emerging Applications
09:50am - 10:50am	**SESSION 8A:** Machine Learning in Test	**SESSION 8B:** Hot Topic: Machine Learning for Test and Diagnosis	**IP SESSION 8C:** Challenges, Opportunities, and Solutions to Hardware Security
11:10am - 12:40pm	**SESSION 9A:** Test Data Analysis	**SESSION 9B:** New Topic: Quantum Systems: Next Challenges in Design,Test, Integration	**SESSION 9C:** TTTC 's E. J. McCluskey Doctoral Thesis Award
12:40pm - 02:00pm	LUNCH		
02:00pm - 03:00pm	**SESSION 10A:** Reliability, Security, Diagnosis	**SESSION 10B:** Hot Topic: Machine Learning and Big Data in Test	**IP SESSION 10C:** Design & Test fo Flexible Hybrid Electronics
02:00pm - 03:00pm	**SESSION 10D:** Town-Hall Meeting for NSF Student Program Participants		

Organizer: *N. Karimi (U. of Maryland Baltimore County)*
Moderator: *N. Karimi (U. of Maryland Baltimore County)*
Named after the late Prof. E.J. McCluskey, a key contributor to the field of test technology, the 2018 TTTC's Doctoral Thesis Award serves the purpose to i) promote the most impactful doctoral student work, ii) provide the students with the exposure to the community and the prospective employers, and iii) support interaction between academia and industry in the field of test technology. TTTC's E.J. McCluskey Best Doctoral Thesis Award will be given to the winning student of the doctoral student contest and his or her advisor. The award consists of a certificate, an honorarium and an invitation to submit a paper on the presented work to the IEEE Design & Test magazine.

The contest is held in two stages: semi-finals and finals: In 2018, semifinals will be held at the IEEE VLSI Test Symposium (VTS), the IEEE European Test Symposium (ETS), the IEEE Latin American Test Symposium (LATS) and the Asian Test Symposium (ATS). The semi-final winners will compete against each other in the finals, held at the International Test Conference (ITC) 2018.

VTS 2018 Semifinalists:
1.Suvadeep Banerjee (Georgia Institute of Technology), **Advisor:** Abhijit Chatterjee
Thesis title: State-Space Encoding Driven Error Resilience in Control Systems And Circuits

2. Mohammad-Mahdi Bidmeshki (University of Texas at Dallas), **Advisor:** Yiorgos Makris
Thesis title: Proof-Carrying Hardware Intellectual Property (PCHIP): Framework Automation and Enhancement

3. Saurabh Gupta (Southern Methodist U.), **Advisor:** Jennifer Dworak
Thesis title: Improving System-on-Chip Test Networks for: Bandwidth, Security, and Power

4. Abhishek Koneru (Duke U.), **Advisor:** Krishnendu Chakrabarty
Thesis title: Test and Reliability Solutions for Monolithic 3D Integrated Circuits

5.Kiruba Sankaran Subramani (U. of Texas at Dallas), **Advisor:** Yiorgos Makris
Thesis title: Hardware Trojans in Wireless Networks

6. Muhammad Yasin (New York U.), **Advisor:** Ozgur Sinanoglu
Thesis title: Provably Secure Logic Locking for Hardening Hardware Security

7. Liwei Zhou (U. of Texas at Dallas), **Advisor:** Yiorgos Makris
Thesis title: Hardware-based Workload Forensics and Malware Detection in Microprocessors

With generous support from the National Science Foundation, 11 US-based Masters or early-Ph.D. students who are neither authors nor presenters have been invited to participate at IEEE VTS'18. The objective of this program, which covers conference registration, lodging and partial travel costs, is to introduce these students to leaders from industry, academia, and government, and expose them to a series of organized and impromptu discussions regarding career trajectories and opportunities in the area of VLSI testing. The following applicants have been selected:

Student Name	Affiliation	Advisor
Md Mahabubul Alam	Pennsylvania State University	Dr. Swaroop Ghosh
Jeremy Blackstone	University of California San Diego	Dr. Ryan Kastner
Arjun Chaudhuri	Duke University	Dr. Krishnendu Chakrabarty
Danielle Duvalsaint	Carnegie Mellon University	Dr. Shawn Blanton
Christopher Nigh	University of California San Diego	Dr. Alex Orailoglu
Elbruz Ozen	University of California San Diego	Dr. Alex Orailoglu
Lakshmi Ramakrishnan	Southern Methodist University	Dr. Jennifer Dworak
Nisharg Shah	Southern Methodist University	Dr. Jennifer Dworak
Shiva Shankar	The University of Texas at Dallas	Dr. Yiorgos Makris
Ashkan Vakil	George Mason University	Dr. Avesta Sasan
Shakil Mahmud	University of South Florida	Dr. Robert Karam

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The Ph.D. Forum at VTS is a poster session for Ph.D. students to present and discuss their dissertation research to a broad audience in the system design and testing community from both industry and academia. The eligible participants includes PhD students who (i) has at least one published or accepted conference, symposium or journal paper ; (ii) will finish their Ph.D. thesis within 1-2 years ; or (iii) has finished his/her PhD thesis during the last academic year.

Student Name	Affiliation	Advisor
Sarani Bhattacharya	Indian Institute of Technology Kharagpur, India	Dr. Debdeep Mukhopadhyay
Mohammad-Mahdi Bidmeshki	University of Texas at Dallas	Dr. Yiorgos Makris
Urbi Chatterjee	Indian Institute of Technology Kharagpur, India	Dr. Debdeep Mukhopadhyay
Abhishek Koneru	Duke University	Dr. Krishnendu Chakrabarty
Deepak Krishnankutty	University of Maryland Baltimore County	Dr. Chintan Patel
Debapriya Basu Roy	Indian Institute of Technology Kharagpur, India	Dr. Debdeep Mukhopadhyay

NOTES

FRINGE MEETINGS

A number of TTTC professional groups interested in test will hold their meetings at VTS 2018. At press time, the following meetings were scheduled. These meetings are for members. If you would like to attend, please contact the person listed at the e-mail address given. Unless specified, all fringe meetings will be held in the Pompeian IV room.

Monday April 23rd	
*12:10 pm - 1:40 pm	**Test Week Workshop Coordination** Yervant Zorian (zorian@synopsys.com)
01:30 pm - 02:15 pm	**TTTC Tutorials and Education Group** Paolo Bernardi (paolo.bernardi@polito.it)
02:15 pm - 03:00 pm	**TTTC Executive Committee** Chen-Huan Chiang (chen-huan.chiang@intel.com)
05:00 pm - 06:00 pm	**TTTC Senior Leadership Board** Yervant Zorian (zorian@synopsys.com)
**06:30 pm - 08:30 pm	**IEEE VTS Technical Program Committee** Amit Mazumdar (amit.majumdar@xilinx.com) Mehdi Tahoori (tahoori@ira.uka.de)

Tuesday April 24th	
09:00 am - 10:00 am	**TTTC Technical Meetings Review Committee** Xiaowei Li (lxw@ict.ac.cn)
10:00 am - 11:00 am	**ITRS DFT SubTeam** Yervant Zorian (zorian@synopsys.com)
*12:10 pm - 01:30 pm	**TTTC Standards Group** Rohit Kapur (rohit.kapur@synopsys.com)
*12:10 pm - 01:30 pm	**Int'l On-Line Test Symposium Committee** Dimitris Gizopoulos (dgizop@di.uoa.gr)

Wednesday April 25th	
10:00 am - 11:00 am	**IEEE VTS Organizing Committee** Chen-Huan Chiang (chen-huan.chiang@intel.com)

**Meeting During Lunch Break*
***Meeting During Dinner in Jeremiah O'Brien Room (By invitation only).*